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REMARKS

Claims 1-29 are currently pending in the subject application and are presently under consideration. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

II. Rejection of Claims 1-29 Under 35 U.S.C. §103(a)

Claims 1-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Miller *et al.* (US 6,643,557) in view of the acknowledged prior art and Moslehi (US 5,719,495). Applicants' representative respectfully requests that this rejection be withdrawn for at least the following reasons. The cited references, neither alone nor in combination, teach or suggest all limitations set forth in the subject claims.

To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, *the prior art reference (or references when combined) must teach or suggest all the claim limitations.* See MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art and not based on the Applicant's disclosure. See *In re Vaack*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). An examiner cannot establish obviousness by locating references which describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent applicant has done. *Ex parte Levengod*, 28 USPQ2d 1300 (P.T.O.B.A.&L 1993). (emphasis added).

Applicants' claimed invention relates to regulation of etching for multi-sloped features (e.g., T-top gate structures, multiple level interconnections and the like) associated with semiconductors. In particular, independent claims 1, 8, 12-15, 25, and 29 recite similar limitations, namely *in-situ regulation of an etch process employed in fabricating a multi-sloped*

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semiconductor feature on a wafer. The cited references are silent regarding such novel aspects of applicants' claimed invention.

Miller *et al.* teaches a general system for using scatterometry to perform feedback and feed forward control on semiconductor devices. A feedback and/or feed-forward modification of the processing of a semiconductor device is carried out in response to a determination that error data collected from a semiconductor processing system merits modification to the processing of semiconductor devices. As noted in the Office Action dated September 10, 2004, Miller *et al.* fails to teach the *measurement of multi-sloped semiconductor features*. The Examiner references a portion of Miller *et al.* that notes "Feedback modification of the control input signal on the line 120 can also be performed on etch processes, such as etch line shape adjustments using etch recipe modifications." (col. 5, lines 19-21, col. 8, lines 14-16). The Office Action incorrectly equivocates feedback modifications such as "line shape adjustments" with *regulating the fabrication of multi-sloped semiconductor features* as in applicants' claimed invention. The "line shape adjustments" to which the Examiner refers do not relate to multi-sloped semiconductor features. The reference merely teaches using feedback control to correct the alignment and direction/shape of the lines. The cited reference is limited to a two-dimensional regulation of semiconductor fabrication and does not teach or suggest modifying an etch process to control a three-dimensional aspect (*e.g.*, slope) of a semiconductor feature as in applicants' claimed invention.

The Examiner attempts to utilize Moslehi to rectify the deficiencies presented by Miller *et al.* Moslehi relates to an apparatus for non-invasive *in-situ* measurements of physical properties of metal, semiconductor wafer surface roughness, and semiconductor surface reflectance. Moslehi does not *teach or suggest in-situ* measurements on *multi-sloped semiconductor features*, and (like Miller *et al.*) is directed to two-dimensional aspects of semiconductor features rather than three-dimensional features as in the claimed invention.

In view of the foregoing, it is readily apparent that none of the references teach or suggest controlling an etch process in connection with multi-sloped semiconductor fabrication; and the mere mention of employment of scatterometry techniques in applicants' specification does not cure the deficiencies of these references.

Accordingly, this rejection with respect to independent claims 1, 8, 12-15, 25, and 29 (and claims that depend there from), should be withdrawn.

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Conclusion

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP660US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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